11 Testing of Logic Circuits

- Fault Model
  - Stuck-At Model
    The model assumes that all faults manifest themselves as some wires (inputs or outputs of gates) being permanently stuck at logic value 0 or 1.
    - The wire \( w \) is stuck-at-0 (denoted as \( w = 0 \)).
    - The wire \( w \) is stuck-at-1 (denoted as \( w = 1 \)).

- Single and Multiple Faults
  Practice has shown that a set of tests that can detect all single faults can also detect the vast majority of multiple faults.

- Complexity of a Test Set
  - Testing combinational circuit
    - The output depends only on the test set.
    - A test set comprised of all possible input valuations (\( 2^n \) for an \( n \)-input circuit) is only suitable for small circuits.
    - A complete test set, capable of detecting all single faults, usually comprises a much smaller number of tests.

- Path Sensitizing
  - Sensitize a path
    Activate a path so that the changes (faults) in the signal that propagates along the path have a direct impact on the output signal.
    - For an AND or NAND gate, all other inputs must be set to 1.
    - For an OR or NOR gate, all other inputs must be set to 0.

The test \( w_1 w_2 w_3 w_4 = 1101 \) detects the occurrence of faults \( a/0, b/0, \) and \( c/1 \).
The test \( w_1 w_2 w_3 w_4 = 0011 \) detects the occurrence of faults \( a/1, b/1, \) and \( c/0 \).

The test set \( (001, 010, 011, 100) \) is used to detect faults in the circuit.
11.4 Circuits with Tree Structure

Figure 11.5 Circuit with a tree structure

11.5 Random Tests

Total number of possible functions of \( n \) variables: \( 2^n \)

<table>
<thead>
<tr>
<th>Test</th>
<th>( f_0 )</th>
<th>( f_1 )</th>
<th>( f_2 )</th>
<th>( f_3 )</th>
<th>( f_4 )</th>
<th>( f_5 )</th>
<th>( f_6 )</th>
<th>( f_7 )</th>
<th>( f_8 )</th>
<th>( f_9 )</th>
<th>( f_{10} )</th>
<th>( f_{11} )</th>
<th>( f_{12} )</th>
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<tbody>
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<td>0 0 0 0 0 0 1 1 1 1 1 1 1 1 1</td>
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<tr>
<td>01</td>
<td>0 0 0 0 1 1 1 1 0 0 0 0 1 1 1</td>
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<tr>
<td>10</td>
<td>0 0 1 1 0 0 1 1 0 0 1 1 0 0 1</td>
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</tr>
<tr>
<td>11</td>
<td>0 1 0 1 0 1 0 1 0 1 0 1 0 1 0</td>
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</tbody>
</table>

Each fault transforms the XOR circuit into a faulty circuit that implements a function other than XOR.
Random testing works particularly well for circuits with a low fan-in. If fan-in is high, it may be necessary to resort to other testing schemes.

11.6 Testing of Sequential Circuit

- The output depends on both the test set and the states.
- Design for Testability
  - Scan-Path Technique
    1. The operation of the flip-flops is tested by scanning into them a pattern of 0s and 1s and observing whether the same pattern is scanned out.
    2. The combinational circuit is tested by applying test vectors on \( x_P, x_{P'}, y_P, y_{P'} \) and observing the values generated on \( x_{P''}, x_{P'''}, y_{P''}, y_{P'''} \).

11.7 Built-In Self-Test (BIST)

Linear Feedback Shift Registers (LFSRs) are used to generate Pseudorandom Binary Sequence (PRBS) and compress the test results.

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Figure 11.10 Effectiveness of random testing

Figure 11.11 Scan-path arrangement

Figure 11.12 Circuit for Example 11.3

Figure 11.13 The testing arrangement

Figure 11.14 Pseudorandom binary sequence generator (PRBSG)
Effectiveness of the BIST approach
- Longer LFSRs give better results.
- Pseudorandomly generated tests do not have perfect coverage of all possible faults.
- The compression process results in a loss of some information on the test results, such that two distinct output patterns may be compressed into the same signature (aliasing problem).
Boundary Scan
- Suppose that each primary input or output pin on a chip is connected through a D flip-flop and that a provision is made for a test mode in which all flip-flops can be connected into a shift register.
- Then the test information can be scanned in and scanned out using the shift-register path on a single chip.
- Shift registers of all chips on a printed circuit board (PCB) can be connected to form a board-wide shift register for testing purpose.