Linear-logarithmic image sensor with low noise and no flickers

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ABSTRACT

This paper proposes and demonstrates a linear-logarithmic image sensor that can operate in both the linear and logarithmic modes, and exhibits low noise and no flickers. Its pixel is composed of one buried-photodiode, five n-channel MOS transistors, two p-channel MOS transistors, and one capacitor. During the linear mode operation, the pixel behaves the same as the four-transistor one, offering a low dark current and low noise. Also, in the logarithmic mode, it operates in an integrating manner in contrast to the majority of logarithmic-response CMOS image sensors that operate in a continuous manner. Thus it has no flickers and can calibrate the fixed pattern noise using the reference level. A wide dynamic range of 190 dB has been confirmed with a 256 \(\times\) 256-pixel image sensor employing this novel pixel architecture.

Keywords: CMOS image sensor, APS, wide dynamic range, logarithmic response

1. INTRODUCTION

Various approaches have been reported in terms of extending the dynamic range of CMOS image sensors. They can be classified into three categories: multiple-exposure\(^1\)-\(^3\), overflow-control\(^4\),\(^5\), and logarithmic-response\(^6\)-\(^17\) methods. As the light intensity in a typical scene encountered in an outdoor environment varies over a range of six decades, and the interscene range will be more than the above mentioned intrascene one, logarithmic response seems to be an essential method to realize an iris-less camera system\(^18\). However, most logarithmic-response image sensors have suffered from a poor performance at low light levels. On the contrary, conventional CMOS image sensors have improved their performance at low light levels by utilizing the four-transistor (4T) pixel\(^19\) which incorporates the buried-photodiode\(^20\). Another drawback of them is that they output a logarithmically converted value of the photocurrent only when the signal is read out without integration, resulting in flicker noise. The standard logarithmic-response circuit\(^6\) utilizes the sub-threshold characteristic of MOS transistors\(^21\), in which the photocurrent is fed to a MOS transistor operating in weak inversion and continuously converted to a logarithmically proportional voltage. Most logarithmic-response image sensors read out the resulting voltage without using any integration process. By exploiting this characteristic, a random addressable APS with three-transistor pixels was proposed\(^7\). A reset transistor was introduced\(^8\) to add a linear-response region and to improve the speed. Although the output signal always represents the actual illumination as long as the circuit bandwidth is higher than the input frequency of the light stimulus, it causes a loss in the beneficial effect of integration on the signal-to-noise ratio and flicker noise. In addition, they also suffer from fixed pattern noise. Reference levels, which are used to remove the threshold voltage variation in a conventional CMOS image sensor, no more exist as each pixel provides a continuous conversion of the light intensity to a voltage. To calibrate the fixed pattern noise, several methods such as using constant-current source\(^9\)-\(^10\) or charge injection\(^11\)-\(^12\) were proposed. Another approach that incorporates column amplifiers for logarithmic conversion and takes images in both the linear and logarithmic modes of operation was proposed\(^13\). On the other hand, our logarithmic-response image sensors\(^14\)-\(^17\) have incorporated integration capacitors and transistors. They operate in an integrating manner and thus naturally have reference levels. By evolving these pixel configurations and introducing the buried-photodiode, a new cell structure has been realized.

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This paper proposes and demonstrates a linear-logarithmic CMOS image sensor that exhibits low noise and no flickers. It can operate in both the linear and logarithmic modes. In contrast to the majority of logarithmic-response CMOS image sensors, which operate in a continuous manner, it operates in an integrating manner even during the logarithmic mode operation. Thus it has no flickers and can calibrate the fixed pattern noise using the reference level. In the linear mode operation, the pixel behaves the same as the four-transistor one.

2. PIXEL DESIGN

2.1 Pixel configuration

The circuit diagram of the pixel is shown in Fig. 1. The pixel consists of one buried-photodiode (PD), five n-channel MOS transistors (M₁, M₂, M₃, M₆, and M₇), two p-channel MOS transistors (M₄ and M₅), and one capacitor (C). As the n-channel MOS transistor M₁ is for excess charges, the pixel would make up the 4T pixel with an overflow transistor without the two p-channel MOS transistors and the capacitor. It can operate in both the linear and logarithmic modes. During the linear mode operation, the two p-channel MOS transistors make up a source follower amplifier and the capacitor its load. Thus the pixel behaves the same as the 4T one, which provides a low dark current and can removes the kTC noise. During the logarithmic mode operation, the M₂ gate is open and the photo-generated current is always fed to the floating diffusion (FD), and the n-channel MOS transistor M₃ and p-channel MOS transistor M₅ operate in weak inversion. M₃ logarithmically converts the photo-generated current to a voltage, which is fed to the M₅ gate. The M₅ source is connected to the capacitor, where a signal logarithmically proportional to the integrated amount of the photo-generated current is stored. The stored signal is read out via the source follower circuit composed of the n-channel MOS transistor M₆ when selected by the n-channel MOS transistor M₇.

![Fig. 1. Pixel configuration.](image-url)
2.2 Principles of logarithmic integration\textsuperscript{14,15}

The relationship between the gate voltage $V_G$, source voltage $V_S$, and the drain current $I_D$ of a MOS transistor in weak inversion is given by

$$I_D = I_{D0} \exp\left(\frac{q}{nkT} (V_G - V_S - V_T)\right)$$

(1)

where $k$, $T$, and $q$ are constants, $n$ is the sub-threshold slope factor of the MOS transistor, $I_{D0}$ is the $I_D$ at the onset of the weak inversion, and $V_T$ is the threshold voltage.

Fig. 2 represents the two basic circuits of logarithmic integration. Here a photodiode is connected to the source or drain of the MOS transistor $M_1$. The other MOS transistor $M_2$ takes care of the integration together with a capacitor $C$.

In Fig. 2 (a), based on the Eq. (1) photocurrent $I_P$ is given by

$$I_P = I_{D0} \exp\left(\frac{q}{nkT} V_{IN} - V_T\right)$$

(2)

when $M_1$ operates in weak inversion. If $M_2$ has the same characteristics as those of $M_1$, and operates in weak inversion, the following equation is derived:

$$C \frac{dV_{OUT}}{dt} = I_{D0} \exp\left(-\frac{q}{nkT} (V_{IN} - V_{OUT} - V_T)\right).$$

(3)
From Eqs. (2) and (3), the following relation is obtained:

\[
\exp\left[\frac{-q}{nkT}V_{\text{OUT}}\right]dV_{\text{OUT}} = \frac{I_p}{C} dt.
\]  \hspace{1cm} (4)

Integrating Eq. (4), assuming \(V_{\text{OUT}}=0\) at \(t=0\), yields

\[
V_{\text{OUT}} = \frac{nKT}{q} \ln\left[\frac{q}{nkTC} \int I_d dt + 1\right]
\approx \frac{nKT}{q} \ln\left[\frac{q}{nkTC} \int I_d dt\right].
\]  \hspace{1cm} (5)

Eq. (5) shows that \(V_{\text{OUT}}\) is logarithmically proportional to the integrated amount of the photocurrent. Note that \(V_{\text{OUT}}\) is proportional not to the integrated amount of the logarithmic value of the photocurrent, but to the logarithmic value of the integrated amount of the photocurrent. This is a very important feature of this circuit because we can easily get a proportional value to the integrated amount of the photocurrent by converting the output value to an exponential.

In the case represented by Fig. 2 (b), the M1 gate is connected to a DC voltage of \(V_R\). \(V_{\text{OUT}}\) is then given by

\[
V_{\text{OUT}} \approx V_{\text{DD}} - \frac{nKT}{q} \ln\left[\frac{aq}{nkTC} \int I_d dt\right],
\]  \hspace{1cm} (6)

assuming that \(V_{\text{OUT}}\) equals \(V_{\text{DD}}\) at \(t=0\), and both transistors have the same value of \(n\). Here \(a\) is the constant defined by the characteristics of the transistors and \(V_R\).

### 2.3 Logarithmic mode operation

There are two methods to reset FD: one is by raising the gate voltage of the transistor \(M_3\) and the other is by lowering its drain voltage, momentarily for both cases. The latter, “fill and spill” method, has been adopted because it makes it possible to correct the threshold voltage variation in the transistor \(M_3\) as well as \(M_5\) by subtracting the output signal before and after the integration\(^{11}\).

Fig. 3 shows the timing diagram for the logarithmic mode operation, along with the transition of the FD node voltage, \(V_{\text{FD}}\), and C node voltage, \(V_C\). In this operation, \(R_{\text{FD}}\) is kept at an intermediate level all the time. During the integration period, the TX pulse is kept at a high level while the OF pulse is low so that the photo-generated charges in the buried-photodiode flow to FD. At \(t=t_1\), which corresponds to the end of the integration period, \(V_C\) is read out as a signal. At \(t=t_2\), TX reaches a low level while OF is high so that the photo-generated charges flow to the overflow drain instead of FD. Meanwhile, charges are injected into FD by lowering RD as shown in (a). When RD returns to the high level at \(t=t_3\), some of the charges begin to return to the drain of the transistor \(M_3\) as shown in (b). As \(M_3\) operates in strong inversion followed by weak inversion, \(V_{\text{FD}}\) rises toward a voltage where \(M_3\) is in the off-state as shown in (c). At \(t=t_4\), \(R_{\text{C}}\) reaches a low level and the transistor \(M_4\) discharges the capacitor. At \(t=t_5\), \(R_{\text{C}}\) returns to a high level, and \(M_4\) become in the off-state. As the transistor \(M_4\) operates in strong inversion followed by weak inversion, \(V_C\) decreases to a voltage where \(M_5\) goes into the off-state. At \(t=t_6\), \(V_C\) is read out as a reference. This reference voltage is subtracted from the signal to remove the threshold voltage variation in the transistor \(M_3\) and \(M_5\). The individual pixel offsets are corrected by subtracting the output signal before integration from one after integration. It is also expected that the random noise is decreased the same as in the case of the soft-reset for the 3T pixel\(^{23}\). At \(t=t_7\), TX returns to a high level while OF is low, and the photo-generated charges begin to flow to FD to start the next integration period.
Fig. 3. Timing diagram and node voltage for logarithmic mode.

Fig. 4. Channel potential for logarithmic mode at selected times: (a) $t=t_2-t_3$, (b) $t=t_3-t_4$, (c) $t=t_6$, and (d) $t=t_7$. 
Fig. 5. Timing diagram and node voltage for linear mode.

Fig. 6. Channel potential for linear mode at selected times: (a) $t = t_2\sim t_3$, (b) $t = t_4$, (c) $t = t_5\sim t_6$, and (d) $t = t_7$. 
As M₃ is already operating in weak inversion without photo-generated charges, the integration period starts with a logarithmic response if V_FD remains intact. However, the response is linear at the beginning if V_FD has become higher with an offset due to the leading edge of the capacitively coupled TX. During this period, M₃ is in the off-state, and V_C tracks V_FD as M₅ operates in weak inversion. As more and more signal charges accumulate on FD, V_FD returns to the point where M₃ begins to operate in weak inversion. After that, a logarithmic integration is performed by M₅ and the capacitor.

### 2.4 Linear mode operation

Fig. 5 shows the timing diagram for the linear mode operation, along with the transition of V_FD and V_C. From t=t₁ to t=t₈, RS_FD is kept at an intermediate level so that the transistor M₄ operates as a load of the source follower circuit linked with M₅. During this period, V_C tracks V_FD. From t=t₂ to t=t₃, FD is reset and RS_FD is kept at a high level. From t=t₅ to t=t₆, charges photo-generated and accumulated in the buried-photodiode are transferred to FD. V_C is read out as a reference at t=t₄, and as a signal at t=t₇. Fig. 6 shows the channel potential around PD and FD at selected times. The KTC noise can be removed by subtracting the potential on the FD node before and after the signal charges are transferred to it. The pixel behaves the same as the 4T one except for a source follower circuit and a capacitor inserted between the FD and the readout amplifier.

### 3. PERFORMANCE

#### 3.1 Test device configuration

A linear-logarithmic CMOS image sensor employing this new pixel architecture was designed and fabricated. The total pixel count is 296 horizontally and 260 vertically, and the effective pixel count is 256 horizontally and 256 vertically. The pixel size is 12.0 × 12.0 µm², and was fabricated using a 0.18 µm 1P4M CIS process.

The following characteristics were measured with an exposure time of 1/30 s.

#### 3.2 Noise characteristics

To clarify the lower limit of the dynamic range of the sensor, its noise was measured for the logarithmic and linear mode operation. For the logarithmic mode operation, the input-referred voltage of the random noise (RN) and fixed pattern noise (FPN) was 0.96 mV rms and 2.6 mV rms, respectively. The FPN is reduced due to the subtraction of the reference from the signal. For the linear mode operation, the input-referred voltage of the RN and FPN was 0.47 mV rms and 2.2 mV rms, respectively.

#### 3.3 Photoelectric conversion characteristics

Fig. 7 shows the photoelectric conversion characteristic for the logarithmic mode operation. The sensitivity is 60 mV/decade. The measurement was carried out using a light box and the sun. The sun was focused on the device via an F1.4 lens for the intensities over 10⁴ lx. Beyond an intensity of about 1.6 × 10⁷ lx, the output signal begins to decrease and the brightest spots turn gray. We suppose this is due to the leakage of photocurrent to FD during the reset operation and can be addressed by enhancing the light shield. If we regard this point as the upper limit of the dynamic range of the sensor, the sensor has a maximum light intensity of 1.6 × 10⁷ lx. On the other hand, the lower limit of the dynamic range for the logarithmic mode operation is 0.0099 lx, which is deduced from the RN of 0.96 mV rms.

Fig. 8 shows the photoelectric conversion characteristic for the linear mode operation. The sensitivity is 9.7 V/lx·s. As the RN for this mode is 0.47 mV rms, the sensor has a minimum light intensity of 0.0048 lx.
Fig. 7. Photoelectric conversion characteristic for logarithmic mode.

Fig. 8. Photoelectric conversion characteristic for linear mode.
3.4 Dynamic range

For the logarithmic mode operation, the dynamic range is 184 dB as the maximum and minimum light intensities are $1.6 \times 10^7$ lx and 0.0099 lx, respectively. On the other hand, the minimum light intensity for the linear mode operation is 0.0048 lx. The dynamic range is extended to 190 dB if the two output signals are stitched.

Fig. 9 presents a reproduced image by the sensor operating in the logarithmic mode. The image was taken by a lens with an aperture of F11 and an exposure time of 1/30 s. The sensor performance is summarized in Table 1.

![Rounded corner image](image-url)

Fig. 9. Reproduced image of a resolution chart and an incandescent lamp.
Table 1. Sensor Performance

<p>| | |</p>
<table>
<thead>
<tr>
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</tr>
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<tbody>
<tr>
<td>Chip Size</td>
<td>5.0 × 5.0 mm²</td>
</tr>
<tr>
<td>Process Technology</td>
<td>0.18 µm 1P4M CIS</td>
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<tr>
<td>Pixel Size</td>
<td>12 × 12 µm²</td>
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<tr>
<td>Fill Factor</td>
<td>38 %</td>
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<tr>
<td>Number of Pixels</td>
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<tr>
<td>Effective</td>
<td>256 × 256</td>
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<tr>
<td>Total</td>
<td>296 × 260</td>
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<tr>
<td>Sensitivity</td>
<td></td>
</tr>
<tr>
<td>Logarithmic Mode</td>
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<tr>
<td>Linear Mode</td>
<td>9.7 V/lx·s</td>
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<tr>
<td>Random Noise</td>
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<td>Logarithmic Mode</td>
<td>0.96 mVrms</td>
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<tr>
<td>Linear Mode</td>
<td>0.47 mVrms</td>
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<tr>
<td>Fixed Pattern Noise</td>
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<tr>
<td>Logarithmic Mode</td>
<td>2.6 mVrms</td>
</tr>
<tr>
<td>Linear Mode</td>
<td>2.2 mVrms</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td></td>
</tr>
<tr>
<td>Logarithmic Mode only</td>
<td>184 dB</td>
</tr>
<tr>
<td></td>
<td>(9.9 × 10⁻³ – 1.6 × 10⁷ lx)</td>
</tr>
<tr>
<td>Logarithmic + Linear Mode</td>
<td>190 dB</td>
</tr>
<tr>
<td></td>
<td>(4.8 × 10⁻³ – 1.6 × 10⁷ lx)</td>
</tr>
</tbody>
</table>

4. CONCLUSION

A linear-logarithmic pixel architecture that employs a buried-photodiode and can operate in both the linear and logarithmic modes was proposed and demonstrated. A 256 × 256-pixel image sensor incorporating this novel pixel architecture was successfully implemented. As it operates in a sampled manner even during the logarithmic mode operation, it is free from flickers. Furthermore, FPN is small because the individual pixel offsets are corrected by subtracting the output signal before integration from one after integration. The sensor has a dynamic range of 184 dB in the logarithmic mode operation. The dynamic range is extended to 190 dB using the linear mode operation at the same time. The lower limit of the dynamic range can be extended due to the linear mode operation that makes it possible to incorporate column amplifiers to reduce the random noise. For example, a double-stage noise canceller is reported to drastically reduce the random noise. We think this pixel architecture that can operate both in the logarithmic and linear modes is very versatile for further extending the dynamic range, although a dynamic range of 190 dB at the moment is sufficient for most applications.

REFERENCES


